An all-inversion-region MOST design methodology applied to a ratioless differential LC-VCO

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***Abstract*—This paper presents a general optimization methodology for analog blocks in RF applications, with CMOS nanometer technologies, based on the complete exploration of all-inversion regions of MOS transistor (MOST). The fundamental tool is the systematic use of the MOST g_m/I_D technique and the description of the real behavior of all devices by means of semi-empirical models. To exemplify this technique, the differential ratioless cross-coupled LC-tank voltage controlled oscillator (LC-VCO) circuit is studied. The implemented design flow minimizes the LC-VCO phase noise considering the constraints of current consumption, output common-mode voltage and output amplitude. To verify the method, six LC-VCO were designed and validated by comparing them with the corresponding electrical simulations.**

***Index Terms*—Optimization, Low power, MOST all-inversion regions, Design Methodology, LC-VCOs, RF**

I. Introduction

At present, the demands of low-cost, efficient and quick time-to-market solutions oblige RF designers to use CMOS nanometer technologies as well as accurate design methodologies applied prior to electrical simulations. It is particularly useful to observe the design's trade-offs when low-power constraints exist. This paper presents a general design methodology focused on nanometer technologies for analog RF blocks that provides the electrical elements sizing as well as the design compromises. The circuit used to exemplify the technique is a cross-coupled differential LC-VCO in which nMOS and pMOS transconductances can take different values (ratioless LC-VCO). The design process is established over the exploration in all-inversion regions of the MOST, to find the best working zone.

We distinguish four main steps:

1) **MOST semi-empirical modeling :** The MOST is characterized as function of the g_m/I_D ratio, which defines the MOST inversion region and has a biunivocal relation with the normalized current $i = I_D/(W/L)$ [1], [2], with I_D, W and L the MOST drain current, width and length, respectively. By measurements or simulations, the behavior of a small set of MOST is captured in look-up tables (LUTs). In them, g_m/I_D is related biunivocally with basic MOST characteristics: transconductance g_m, drain-source conductance g_{ds}, drain current I_D, normalized intrinsic capacitances C'_{ij}, with $ij = \{gs, gd, gb, bd, bs\}$ and noise parameters. In this work, these data are extracted via electrical simulation with the information provided by the foundry. As a hypothesis, MOST is considered to be working quasistatically, so its working frequency f_0 is at least one tenth of its transition frequency f_T [3].
2) **Passive semi-empirical modeling :** Parasitic parameters extraction of passive components (inductors, capacitors, varactors and resistors) are expressed in LUTs, for the working frequency f_0. Since for each nominal value of the element, different geometries are possible, only the best devices are included in the LUTs (e.g. devices with the largest quality factor for each nominal value).
3) **Signal and noise analytical modeling :** RF block core characteristics are modeled. When necessary, perform the equations modifications to link them with the device characteristics described in steps 1) and 2).
4) **Design Flow :** Create a simple and systematic design flow where the relations between block equations, extracted parameters and necessary decisions are properly organized, all intended to fulfill the particular specifications of the block and technological process constraints.

The paper is organized as follows. Section II presents the way the CMOS process is modeled, dividing its study in the modeling of MOST and passive components. Section III discuses the design flow of one particular RF circuit: the cross-coupled ratioless differential LC-VCO. Finally come the Conclusions.

II. Modeling of nanometer CMOS processes

A good modeling of the process involved in the design is necessary in order to correctly characterize its active and passive devices. Not doing so would lead to substantial mismatches between the circuit features observed at the design level and after electrical simulation. MOST and passive devices are modeled in this work using: a) semi-analytical models whose parameters are in LUTs and depend on primary electrical magnitudes; and b) semi-empirical models whose data are in LUTs extracted from electrical simulations. These models prove to be enough for RF applications at least until 5 GHz with our RF 1.2-V 90nm CMOS process.

A. MOS transistor model

As a rule of thumb [4], for the 90nm CMOS technology used in this work, weak inversion (WI) is considered for g_m/I_D above 20 V^{-1}, strong inversion (SI) is below

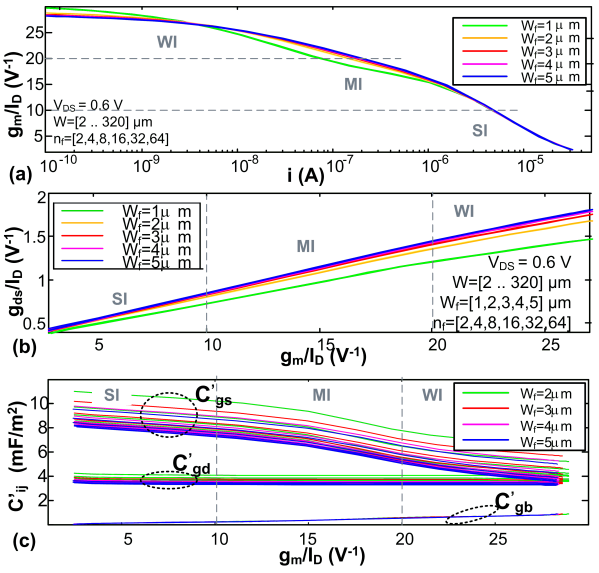

Figure 1. MOST characteristics: (a) g_m/I_D vs. i; (b) g_{ds}/I_D vs. g_m/I_D and (c) C'_{ij} vs. g_m/I_D for a wide set of W.

g_m/I_D=10 V^{-1} and moderate inversion (MI) is in the midst of them, as shown in Fig. 1. Our MOST semi-empirical model (semi-analytical for noise model) comprises LUTs with the following data:

1) g_m/I_D as function of the normalized current i, shown in Fig. 1.(a). The dependency of g_m/I_D with W, V_{DS} is slight and in a first approximation it can be neglected if narrow devices with finger widths W_f <2 μm are discarded.
2) g_{ds}/I_D as function of g_m/I_D and V_{DS}. The variation with W is very slight, as seen in Fig. 1.(b), and it is not considered here.
3) Normalized capacitances C'_{ij} versus g_m/I_D, as seen in Fig. 1.(c). The spread with W and V_{DS} is reasonably small, hence it is not considered in our approximation.
4) Noise parameters: a) thermal noise parameters γ/α [3], as function of g_m/I_D and V_{DS} (variation with W can be neglected in a first approximation); b) flicker noise parameter K_F versus g_m/I_D, at f_0 (dependency with W and V_{DS} is very low and not considered here).
5) Overdrive voltage $V_{OD} = V_{GS} - V_T$ versus g_m/I_D (the spread of V_{OD} with W and V_{DS} is very low and it is not included in our LUTs).

B. Passives model

The semi-empirical passive components' models are obtained via AC electrical simulations. The extraction of these models depends on the topological location of the component; for example, when the device has an AC grounded terminal or when it is fully differential. In Fig. 2, the plots of parallel parasitic resistance of inductance L_{ind} and series parasitic resistance of capacitance C_{cap} are shown for f_0=2.45 GHz. The best devices are marked with a black thick line. The LUT includes, for each best device, the nominal value of the

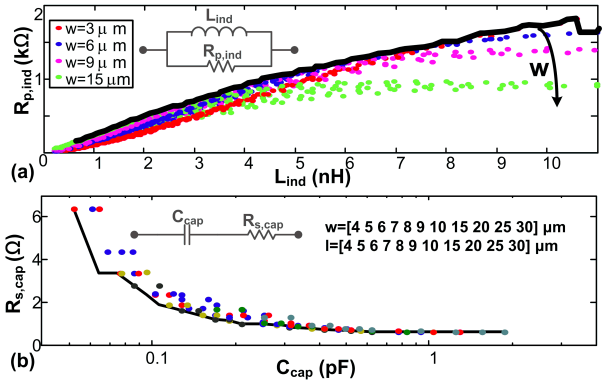

Figure 2. (a) Inductor parallel parasitic resistance $R_{p,ind}$ versus inductance L_{ind} for a wide set of inductors' sizes; and (b) capacitor series parasitic resistance $R_{s,cap}$ vs. capacitance C_{cap} for a wide set of capacitors' size.

element, the associated parasitic and its physical size. Despite this semi-empirical modeling is simple, it gives us good results. The biunivocal relation between the best element's nominal value and its parasitic, e.g. between the inductor inductance and its parasitic serial resistance, is very useful to generate a simple design flow.

III. Design Methodology Applied to an LC-VCO

The implementation of the two last steps of the general methodology of Section I are specific of each analog RF circuit. Here, we choose to study a cross-coupled differential LC-VCO, sketched in Fig. 3. Its special feature is that it is a ratioless VCO, i.e. its nMOS and pMOS small-signal transconductances $g_{m,n}$ and $g_{m,p}$ are not equal. Since both transistors join the drain current I_D, $(g_m/I_D)_n \neq (g_m/I_D)_p$. As g_m/I_D indicates the MOST inversion region, nMOS and pMOS transistors are in different inversion regions.

The design methodology here presented extends the work of the authors in [2], where these transconductances were considered identical (ratioed LC-VCO). The removal of this bound permits to adjust the output amplitude voltage A_{out}, common-mode output voltage $V_{o,cm}$ and phase noise playing with nMOS and pMOS coupled-pairs $(g_m/I_D)_n$ and $(g_m/I_D)_p$ ratios. To implement this idea, we use an analytical LC-VCO small-signal modeling, resumed next.

A. LC-VCO signal modeling

Oscillation frequency and oscillation condition are

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind}C_{tank}}}$$
$$g_{tank} = (g_{m,n} + g_{m,p})/(2\ k_{osc}) \quad (1)$$

with k_{osc} the oscillation safety factor. Assuming that the inductor parasitic conductance g_{ind} is much higher than the varactor one (as the varactor parallel parasitic resistance is around 20 kΩ), the tank capacitance and tank conductance are

$$C_{tank} = C_{var} + \frac{C_{MOS,n} + C_{MOS,p}}{2} + C_{load} \quad (2)$$
$$g_{tank} = g_{ind} + \frac{g_{ds,p}}{2} + \frac{g_{ds,n}}{2} \quad (3)$$

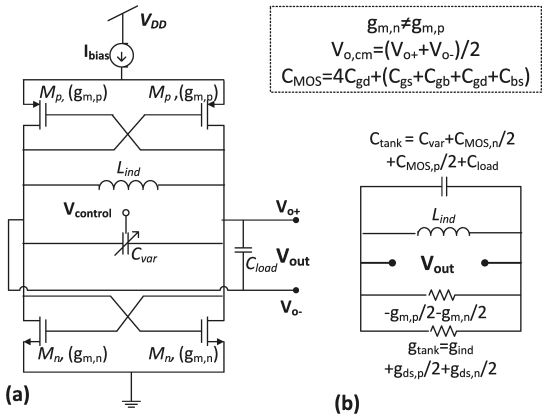

Figure 3. VCO (a) schematic and (b) small-signal equivalent circuit.

with $C_{MOS,n(p)}$ the cross-coupled nMOS (pMOS) effective capacitance (see Fig. 3), and C_{var} and C_{load} the varactor and load capacitances. The drain current is

$$I_D = \frac{2g_{ind}}{(g_m/I_D)_n \; 1/k'_{osc,n} + (g_m/I_D)_p \; 1/k'_{osc,p}}. \quad (4)$$

with $k'_{osc,n(p)} = (1/k_{osc} - g_{ds,n(p)}/g_{m,n(p)})^{-1}$. The output amplitude voltage is [5]

$$A_{out} \cong \frac{8}{\pi} \frac{2k_{osc}}{(g_m/I_D)_n + (g_m/I_D)_p}, \quad (5)$$

and $V_{o,cm}$, obtained using [6], depends on I_D, A_{out} and the nMOS transistor aspect ratio.

Finally, the phase noise model of this structure in the white noise zone when $g_{m,n} \neq g_{m,p}$ is derived similarly as in [2], and results in

$$\mathcal{L} = 10log\left(k_B T \frac{\pi^2}{32} \frac{\Gamma^2_{rms}}{Q^2_{tank} I_D} \left(\xi_n \left(\frac{g_m}{I_D} \right)_n + \xi_p \left(\frac{g_m}{I_D} \right)_p \right) \frac{f_0^2}{\Delta f^2} \right). \quad (6)$$

where k_B is the Boltzmann constant, T is the absolute temperature, Q_{tank} the tank quality factor (with $Q_{tank} = (\omega_0 L_{ind}, g_{tank})^{-1}$), Γ is the Impulse Sensitive Function [7], f_0 is the oscillation frequency, Δf is the offset frequency and $\xi_{n(p)} = \frac{1}{2}\left(\left(\frac{\gamma}{\alpha}\right)_{n(p)} + \frac{1}{k_{osc}} \right)$. The ratio γ/α is the thermal noise parameter which depends on g_m/I_D, as we stated in Section II-A.

B. Design methodology flow

This subsection details the proposed design flow developed here to implement the last step of the methodology introduced in Section I. This design flow systematically obtains the set of LC-VCOs that minimizes the phase noise for each $(g_m/I_D)_n$, with constraints in current consumption, output common-mode voltage $V_{o,cm}$ and output amplitude A_{out}. For the sake of simplifying the explanation, the optimization process is implemented exhaustively in the whole design domain, being it all the feasible inductors $L_{ind} \in \Phi_{Lind}$ and all the nMOS transistor inversion levels $(g_m/I_D)_n \in \Phi_{gmID,n}$. From (4) and (6), to limit the increment of current consumption when the phase noise is minimized, we consider $(g_m/I_D)_p$ a thirty percent away from $(g_m/I_D)_n$, that is $(g_m/I_D)_p \in (g_m/I_D)_n \cdot [0.7, 1.3] = \Psi_{n,30\%}$.

The corresponding design flow is organized as follows:

1) Start fixing a set of initial parameters: minimum transistor channel length L_{min}, k_{osc}, maximum equivalent inductance $L_{ind,max}$, minimum varactor capacitance $C_{var,min}$, C_{load}, and grids of $\Psi_{n,30\%}$, $\Phi_{gmID,n}$ and Φ_{Lind}. Next, set the VCO specifications: f_0, maximum current $I_{D,max}$, maximum phase noise $\mathcal{L}_{max}$ at an offset Δf, minimum output amplitude $A_{out,min}$ and $V_{o,cm} \in [V_{o,cm,min}, V_{o,cm,max}]$ [6].
2) Pick $L_{ind,i}$ and $(g_m I_D)_{n,k}$ from Φ_{Lind} and $\Phi_{gmID,n}$.
3) From the inductor LUT, derive g_{ind} of $L_{ind,i}$.
   Obtain i_n, $(g_{ds}/I_D)_n$ and $C'_{ij,n}$ from the picked $(g_m/I_D)_{n,k}$ and the nMOS transistor LUTs.
   For each $(g_m/I_D)_{p,j}$ of $\Psi_{n,30\%}$ calculate the drain current $I_{D,j}$ from (4). Obtain $i_{p,j}$ and compute $W_{n,j}$ and $W_{p,j}$ from i_n, $i_{p,j}$ and $I_{D,j}$. Compute $g_{ds,n(p)}$ from the MOST LUTs. Finally, with (1) and (2) calculate Q_{tank} and C_{var}.
   Compute $V_{o,cm}$, A_{out} and $\mathcal{L}$ from [6], (5) and (6), respectively.
   If $I_D > I_{D,max}$, $\mathcal{L} > \mathcal{L}_{max}$, $C_{var} < C_{var,min}$, $V_{o,cm} \notin [V_{o,cm,min}, V_{o,cm,min}]$ or $A_{out} < A_{out,min}$ discard this $(g_m/I_D)_p$ and choose another j. If finishing covering all the elements of $\Psi_{n,30\%}$, continue.
4) From all the valid $(g_m/I_D)_p$ found in **3)**, find the $(g_m/I_D)_p$ that minimizes the phase noise $\mathcal{L}$.
5) If all points of $\Phi_{gmID,n}$ are not covered return to **2)** and increase k. Otherwise, find the k^* of $\Phi_{gmID,n}$ that minimizes the phase noise $\mathcal{L}_{ik^*}$. Then, if all points of Φ_{Lind} are not covered return to **2)** and increase i, otherwise the design is finished.

The design flow is implemented in MATLAB routines, with f_0=2.45 GHz, Δf=400 kHz, $I_{D,max}$=0.9 mA, $C_{var,min}$=40 fF, $A_{out,min}$=0.4 V and $V_{o,cm}$=[0.2, 0.6] V. The family of curves of phase noise and power consumption, shown in Figure 4, are obtained for ratioed and ratioless VCOs. It is observed that lowest phase noise values are reached in SI, and highest ones in WI; the contrary happens for power consumption. It is also gathered that lower phase noise and higher current are obtained when nMOS and pMOS transconductances are not equal.

Figure 6 presents the $(g_m/I_D)_p$ color plot versus $(g_m/I_D)_n$ and L_{ind}. As expected, due to (6), the routine chooses the minimum available $(g_m/I_D)_p$ for each $(g_m/I_D)_n$, except when the constraints are not met (for low inductor values). Figure 5 represents the minimum phase noise value achieved for each feasible inductor. For small inductors, some imposed restrictions are reached and the minimum valid $(g_m/I_D)_n$ raises, increasing the chosen $(g_m/I_D)_p$ and, from (6), the corresponding phase noise, as gathered in the inset of Fig. 5.

Table I lists six LC-VCOs in the three inversion regions (SI, MI and WI) for various tank inductors values. The computed

Table I
METHOD VALIDATION: COMPARISON BETWEEN RESULTS FROM MATLAB AND SPECTRERF SIMULATIONS.

Design	$(g_m/I_D)_n$ (1/V)	$(g_m/I_D)_p$ (1/V)	A_{out} (V)		$V_{o,cm}$ (V)		$\mathcal{L}_{@400kHz}$ (dBc/Hz)		L_{ind} (nH)	R_{ind} ($k\Omega$)	I_D (mA)	W_n (μm)	W_p (μm)	C_{var} (pF)
			Calc.	Sim.	Calc.	Sim.	Calc.	Sim.						
PSI1	10	7	0.9	1.16	0.51	0.54	-119.2	-118.2	2.6	0.64	0.73	15.1	25.9	1.36
PSI1	10	7	0.9	1.16	0.51	0.54	-110.6	-111.3	8.7	1.6	0.29	6.0	10.2	0.26
PMI1	16	11.3	0.56	0.72	0.39	0.37	-115.5	-115.3	2.6	0.64	0.45	44.8	41.9	1.27
PMI2	16	11.3	0.56	0.72	0.39	0.37	-113.3	-112.2	5.1	1.12	0.25	25.4	24.0	0.54
PWI1	20	14	0.45	0.58	0.28	0.29	-110.2	-109	5.1	1.12	0.20	115.3	36.0	0.38
PWI2	20	14	0.45	0.58	0.28	0.29	-113.6	-112.6	2.6	0.64	0.35	181	63.3	0.98

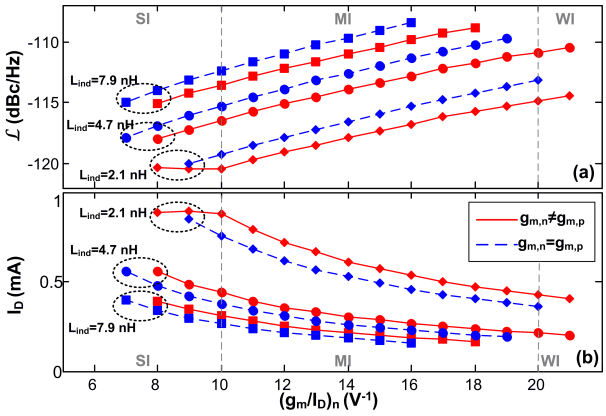

Figure 4. Comparison of (a) phase noise and (b) drain current for three real inductors considering ratioless(continuous line) and ratioed (broken line) VCOs.

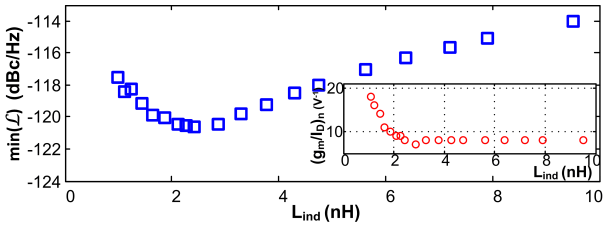

Figure 5. Minimum phase noise obtained from the design flow. The inset shows its corresponding $(g_m/I_D)_n$.

$\mathcal{L}$, A_{out} and $V_{o,cm}$ are compared with the SpectreRF simulated results. As expected, $(g_m/I_D)_p$ value is lower than $(g_m/I_D)_n$ so as to reduce the phase noise. For all designs, phase noise error is lower than 1.2 dB. Finally, for the amplitude and common-mode voltage the relative error is below 10%, which is a very good result if considering the simplifications made in (5).

IV. CONCLUSIONS

This paper presents a general optimization methodology for RF analog blocks implemented in CMOS nanometer technologies which study all-inversion regions of the MOST. Semi-empirical models are used for the process components (MOST, inductors, capacitors, varactors, resistors), obtaining their LUTs from electrical simulations. A differential cross-coupled LC-VCO with ratioless nMOS and pMOS transconductances is used to exemplify the last two steps of the methodology. A design flow that minimizes the phase noise

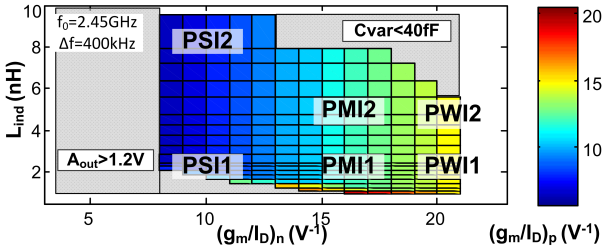

Figure 6. Color plot of $(g_m/I_D)_p$ versus $(g_m/I_D)_n$ and L_{ind}. Zones where constraints are not met are shadowed.

considering power, output amplitude and output common-mode voltages constraints is developed and implemented in MATLAB routines. Trade-offs between designing ratioed and ratioless LC-VCOs are given. Six LC-VCO designs were simulated, whose characteristics match, with an acceptable error, with the computed data.

V. ACKNOWLEDGMENTS

This work has been financed in part by the Junta de Andaluca project P09-TIC-5386 and the Ministerio de Economia y Competitividad project TEC2011-28302, both of them co-financed by the FEDER program.

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